IN THE SPECIFICATION:

Please replace the paragraph that begins on line 1 of page 37 with the following amended paragraph:

Turning now to FIGURE 4, illustrated is a block diagram of an embodiment of a resampler 400 constructed according to the principles of the present invention. The resampler 400, including a front end 401, a filter stage 415 and a combining stage 420, receives first, second and third input signals Rin0, Rin1, Rin2 and provides a resampled output signal Rout. The front end 401 includes a delay stage 402, an interpolation stage 405 and a selection stage 410. The delay stage 402 is coupled to the first, second and third input signals Rin0, Rin1, Rin2, and the interpolation stage 405 is interposed between the delay and selection stages 402, 410~~, and the selection stage 410 is coupled to an oscillator TG1~~. An oscillator TG1 is coupled to the front end 401 including the selection stage 410. The selection stage 410 provides first, second and third front end output signals or samples Rout0, Rout1, Rout2.